WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising:

forming a gate oxide over a substrate and a gate electrode over the gate oxide;

implanting impurities into the substrate using the gate electrode as an implant mask to form lightly-doped regions in the substrate;

forming a first spacer adjacent the gate electrode;

implanting impurities into the substrate and through a portion of the lightly-doped regions using the first spacer as an implant mask to form deep source/drain regions in the substrate;

forming a second spacer adjacent the first spacer;

implanting impurities into the substrate using the second spacer as an implant mask to form a graded source/drain region in the substrate; and

removing the second spacer.

2. The method as recited in Claim 1, wherein said first spacer comprises a nitride.

3. The method as recited in Claim 1, wherein said second spacer comprises an oxide.

4. The method as recited in Claim 3, wherein the second spacer is a low-temperature oxide having a thermal budget of less than 600C.

5. The method as recited in Claim 1, further including depositing a nitride layer over the gate electrode and lightly-doped regions and forming the first spacer from the nitride layer, and further including depositing an oxide layer over the gate electrode and lightly-doped regions and forming the first spacer from the oxide layer.

6. The method as recited in Claim 1, further including forming a salicide over the source/drain regions.

7. The method as recited in Claim 1, further including:

forming a dielectric over the gate electrode and the deep source/drain regions;

forming a contact opening through said dielectric; and

forming an interconnect in said contact opening, the interconnect being electrically coupled to the deep source/drain regions.

8. A method of manufacturing a semiconductor device, comprising:

forming a gate oxide over a substrate and a gate electrode over the gate oxide;

implanting impurities into the substrate using the gate electrode as an implant mask to form lightly-doped regions in the substrate;

forming a first spacer adjacent the gate electrode;

forming a second spacer adjacent the first spacer;

implanting impurities into the substrate using the second spacer as an implant mask to form a graded source/drain region in the substrate;

removing the second spacer; and

implanting impurities into the substrate and through a portion of the lightly-doped regions using the first spacer as an implant mask to form deep source/drain regions in the substrate.

9. The method as recited in Claim 8, wherein said first spacer comprises a nitride.

10. The method as recited in Claim 8, wherein said second spacer comprises an oxide.

11. The method as recited in Claim 10, wherein the second spacer is a low-temperature oxide having a thermal budget of less than 600C.

12. The method as recited in Claim 8, further including depositing a nitride layer over the gate electrode and lightly-doped regions and forming the first spacer from the nitride layer, and further including depositing an oxide layer over the gate electrode and lightly-doped regions and forming the first spacer from the oxide layer.

13. The method as recited in Claim 8, further including forming a salicide over the source/drain regions.

14. The method as recited in Claim 8 further including:

forming a dielectric over the gate electrode and the source/drain regions;

forming a contact opening through said dielectric; and

forming an interconnect in said contact opening, the interconnect being electrically coupled to said source/drain regions.

15. A semiconductor device, comprising:

a gate structure formed over a semiconductor region;

a sidewall spacer formed along a sidewall of the gate structure;

a disposable spacer formed along an outer edge of the sidewall spacer;

a lightly-doped region formed in the semiconductor region to a first depth, the lightly-doped region substantially aligned with the sidewall of the gate structure;

a deep source/drain region formed in the semiconductor region to a second depth deeper than the first depth, the deep source/drain region substantially aligned with an outer edge of the sidewall spacer; and

a graded source/drain region formed in the semiconductor region to a third depth

deeper than the second depth, the graded source/drain region substantially aligned with an outer edge of the disposable spacer.

16. The device as recited in Claim 15, wherein the disposable spacer comprises a low-temperature oxide having a thermal budget of less than 600C.

17. The device as recited in claim 15, wherein the lightly doped region, the deep source/drain region, and the graded source/drain region are formed from impurities of the same conductivity type.

18. The device as recited in claim 17, wherein the lightly doped region, the deep source/drain region, and the graded source/drain region are formed from impurities of the same material.

19. The device as recited in claim 15, further comprising a salicide region formed at the surface of the semiconductor region adjacent the outer edge of the sidewall spacer.

20. The device as recited in Claim 15, wherein the semiconductor region comprises a silicon-on-insulator substrate.